EMR 2721

PCM Signal Conditioner

EMR TELEMETRY DIVISION

TELEMETRY DIVISION EMR

EMR 2721 PCM SIGNAL CONDITIONER

ELECTRO-MECHANICAL RESEARCH, INC. • BOX 3041 • SARASOTA, FLORIDA 33578

EMR 2721 PCM SIGNAL CONDITIONER

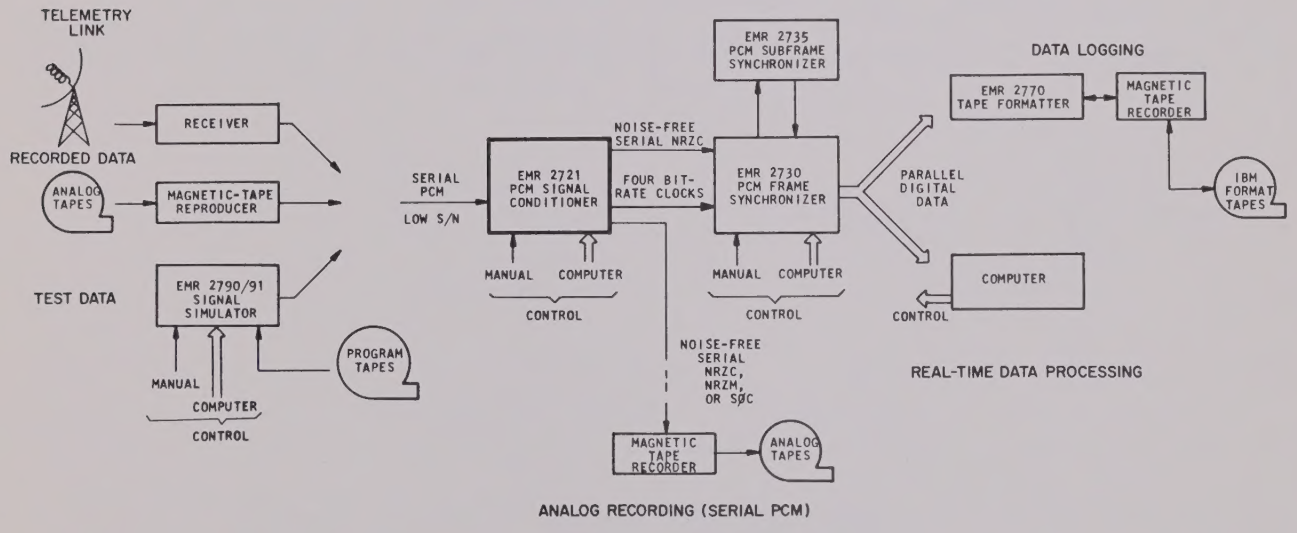
- Computer or manual control by switch setting
- Recovery, reconstruction and bit synchronization
- All codes from 10 bps to 1 Mbps
- Status display for all parameters
- Filter Sample and Reset integrator detectors
- Incorporates analog and digital integrated circuits

GENERAL

The EMR 2721 PCM Signal Conditioner, one of the EMR 2700-Series data processing modules, recovers serial PCM pulse trains in the presence of noise and generates bit-rate clock signals. The unit is a complete subsystem including power supply, input-output connectors, and internal cooling. All functions are contained in one standard 19-inch EIA drawer which requires a panel height of 5-1/4 inches.

SYSTEM APPLICATION

The EMR 2721 operates either with a digital data processing system under computer control or as an independent unit manually programmed by front panel switches. The basic model accepts virtually all types of noisy serial PCM signals, NRZC, NRZM, NRZS, SØC, SØM, SØS, RZ, and bipolar at rates of 10 bps to 1 Mbps, and levels from 500 mv to 30 v. Incoming serial bit streams are reconstructed as a noise-free serial NRZC output accompanied by bit rate clock pulse trains. An additional output is also provided for recording the serial PCM in either NRZC, NRZM, or SØC.



TYPICAL SYSTEM APPLICATIONS

EMR 2721 CONFIGURATION

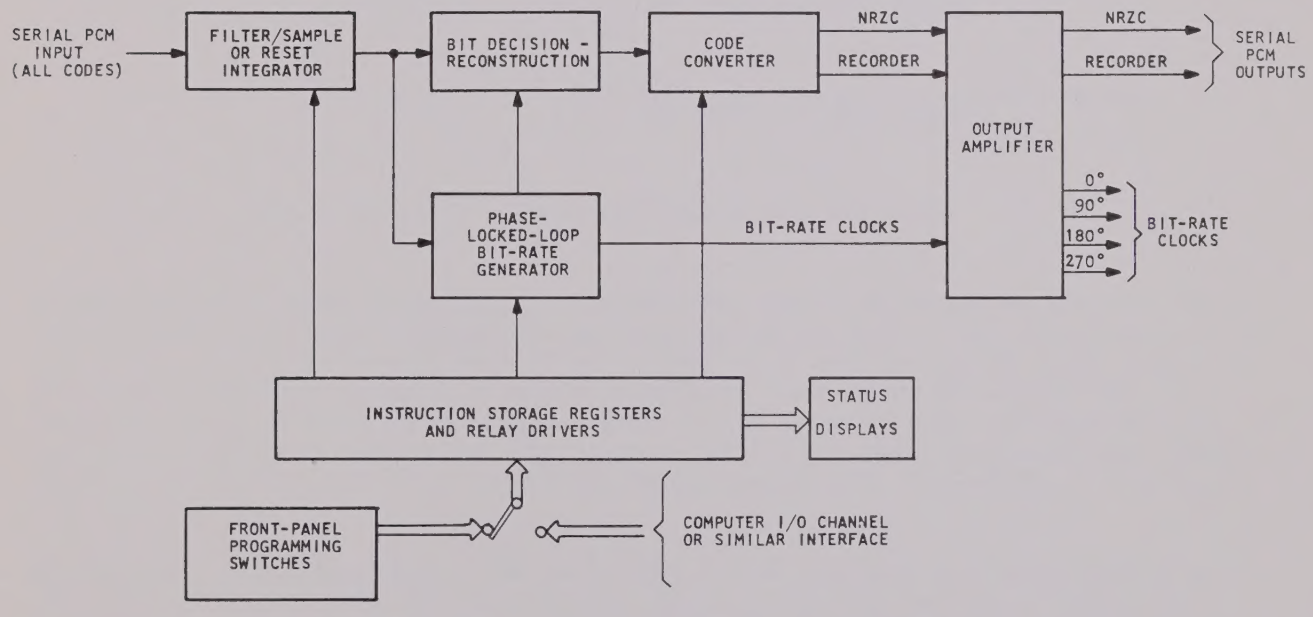
The EMR 2721 PCM Signal Conditioner incorporates a wide range of program-selectable operating characteristics. Functions normally available as options have been economically included in the EMR 2721. For example, either a reset-integrator or a constant time-delay filter can be selected for input signal conditioning.

FUNCTIONAL DESCRIPTION

The overall function of the EMR 2721 PCM Signal Conditioner, which receives operating instructions from either a computer or front panel programming switches, is to accept any desired type of serial pulse-code-modulated (PCM) data at low signal-to-noise ratios and provide reconstructed serial PCM outputs and synchronous bit rate signals.

Operating Instructions Programming

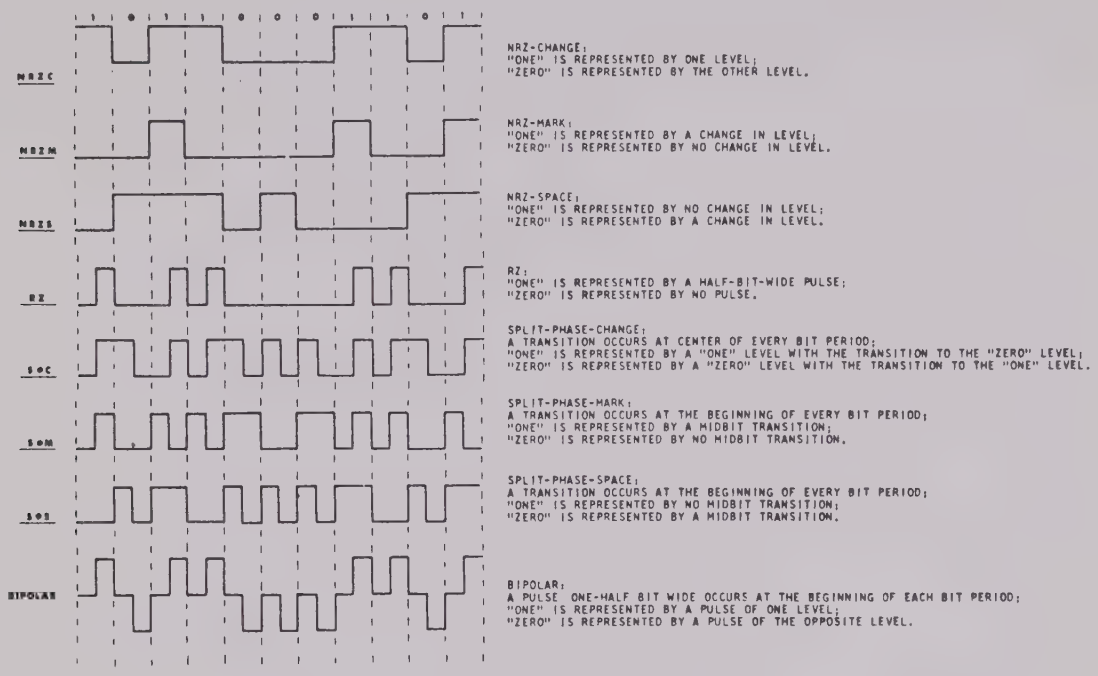
Operating instructions are entered into a designated group of flip-flop storage registers from either front panel programming switches or a computer I/O channel. The programming format is the same for either mode of entry. The contents of the instruction storage registers operate relays which set up the operating configuration of the EMR 2721. The operating status is displayed on the front panel.



EMR 2721 PCM SIGNAL CONDITIONER
BLOCK DIAGRAM

Signal Conditioning and Code Conversion

Input Codes - PCM input codes accepted by the EMR 2721 for conditioning and conversion to fixed output codes (NRZC and either NRZC, NRZM or Split-Phase C for recording) are illustrated below:


1 0 1 1 0 0 1 0 1
NRZC
NRZ-CHANGE;
"ONE" IS REPRESENTED BY ONE LEVEL;
"ZERO" IS REPRESENTED BY THE OTHER LEVEL.
NRZM
NRZ-MARK;
"ONE" IS REPRESENTED BY A CHANGE IN LEVEL;
"ZERO" IS REPRESENTED BY NO CHANGE IN LEVEL.
NRZS
NRZ-SPACE;
"ONE" IS REPRESENTED BY NO CHANGE IN LEVEL;
"ZERO" IS REPRESENTED BY A CHANGE IN LEVEL.
RZ
RZ;
"ONE" IS REPRESENTED BY A HALF-BIT-WIDE PULSE;
"ZERO" IS REPRESENTED BY NO PULSE.
SØC
SPLIT-PHASE-CHANGE;
A TRANSITION OCCURS AT CENTER OF EVERY BIT PERIOD;
"ONE" IS REPRESENTED BY A "ONE" LEVEL WITH THE TRANSITION TO THE "ZERO" LEVEL;
"ZERO" IS REPRESENTED BY A "ZERO" LEVEL WITH THE TRANSITION TO THE "ONE" LEVEL.
SØM
SPLIT-PHASE-MARK;
A TRANSITION OCCURS AT THE BEGINNING OF EVERY BIT PERIOD;
"ONE" IS REPRESENTED BY A MIDBIT TRANSITION;
"ZERO" IS REPRESENTED BY NO MIDBIT TRANSITION.
SØS
SPLIT-PHASE-SPACE;
A TRANSITION OCCURS AT THE BEGINNING OF EVERY BIT PERIOD;
"ONE" IS REPRESENTED BY NO MIDBIT TRANSITION;
"ZERO" IS REPRESENTED BY A MIDBIT TRANSITION.
BIPOLAR
BIPOLAR;
A PULSE ONE-HALF BIT WIDE OCCURS AT THE BEGINNING OF EACH BIT PERIOD;
"ONE" IS REPRESENTED BY A PULSE OF ONE LEVEL;
"ZERO" IS REPRESENTED BY A PULSE OF THE OPPOSITE LEVEL.

SERIAL PCM INPUT CODES ACCEPTED BY THE EMR 2721

Filter/Sample or Reset Integrator - For optimum operation either a constant-time-delay filter or a reset integrator can be selected to extract the PCM signals from the noise. Two filters are used, one for NRZ codes and one for RZ codes since the RZ signal frequency spectrum is twice as wide as that of an NRZ signal of the same bit rate. A phase-sensitive detector in the input circuit translates the split-phase codes to equivalent NRZ signals for better signal-to-noise performance. DC restoration is used after the filtering to reestablish the median of the input PCM signal.

Bit Decision/Reconstruction - The decision circuit consists of a high-gain limiter and shift register. The bit decision is based on whether the input signal is positive-going or negative-going. The PCM signal is reconstructed by gating the shift register circuit with the clock signal from the phase-locked-loop bit-rate generator.

Code Converter - The code conversion circuit provides an NRZC output signal regardless of the input signal code. Either an NRZC, NRZM, or SØC signal is supplied at the proper level for most magnetic tape recorders without the use of special equipment.

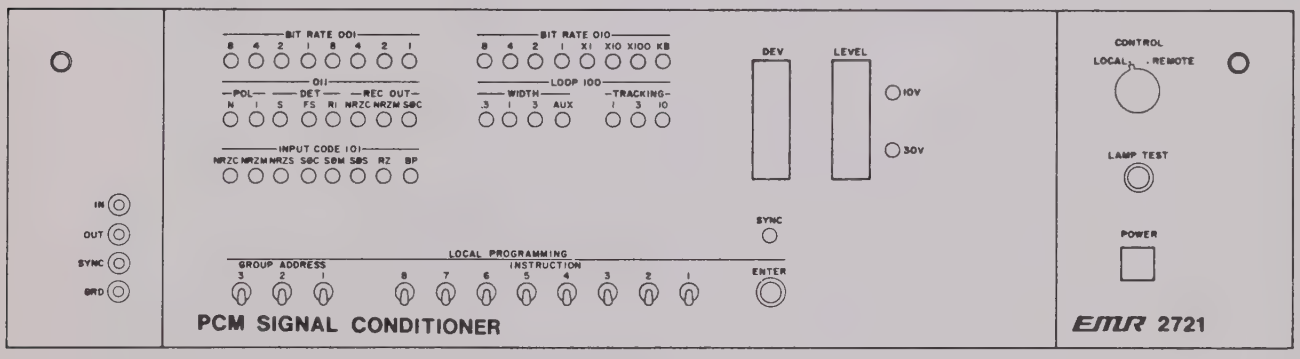
Phase-Locked Loop Bit-Rate Generator - An analog phase-locked loop generates bit-rate clock pulses in synchronism with the reconstructed serial PCM outputs.

Selectable loop widths and tracking ranges provide optimum performance for various conditions. A low-drift loop amplifier and stable VCO provide the accuracy required throughout the bit-rate range. The synchronizer is considered in synchronization when less than one cycle of clock is gained or lost during a data frame of 2000 bits.

Output Amplifier - The output amplifier provides buffering and amplification for the NRZC output, the recorder output (NRZC, NRZM, or SØC), and the four bit-rate clocks at 0^{o}, 90^{o}, 180^{o}, and 270^{o} with respect to the PCM output.

LOCAL/REMOTE CONTROL

The parameters of the EMR 2721 can be controlled either by instructions from a computer, or by instructions entered via programming switches on the front panel. The same programming format is used in either case. A single control switch enables either one of the two sources of control to be used by selecting either the Remote or Local position. Flip-flop storage registers are used to store instructions originating from either source, and the contents of these registers are displayed on the front panel to indicate the operational status of the unit.



MANUAL PROGRAMMING

Instructions can be entered by the front panel programming switches when the EMR 2721 is operated as an independent unit. Alternatively, if the unit is under computer control, computer instructions already entered can be modified at any time without interrupting the computer program.

The manual programming sequence is as follows:

1. Set the CONTROL switch to LOCAL.

2. Program the GROUP ADDRESS switches to the function to be modified. The function name and binary group address are marked on the front panel. For example, the INPUT CODE function group address is 101.

3. Program the INSTRUCTIONS switches to the required function parameter. For example, if it is desired to accept an NRZS input code, the instruction is 00100000

4. Operate the ENTER pushbutton momentarily to store and execute the programmed instruction.

Due to the ease of correlating the programming switch settings with the displays, a programming form or card is not required.

COMPUTER PROGRAMMING

The EMR 2721 can be completely controlled by a computer or other compatible remote device. Remote control permits:

1. Setting up the unit for operation.

2 Controlling all parameters in real time.

3. Performing diagnostic programs.

Remote control is via 16 data lines and one data transfer line. The programming format and intelligence of the 16-bit words consist of:

1. Four lines (13 to 16) for the module address.

2. Four lines (9 to 12) for the group address which determines the function within the EMR 2721 that is being addressed.

3. Eight lines (1 to 8) for the actual instruction.

MODULE ADDRESS				GROUP ADDRESS				INSTRUCTION							
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0	0	0	1	0	0	0	1	8	4	2	1	8	4	2	1
0	0	0	1	0	0	1	0	8	4	2	1	X1	X10	X100	KB
0	0	0	1	0	0	1	1	N	POL I	S	DET FS	RI	NRZC	REC OUT NRZM	SØC
0	0	0	1	0	1	0	0	.3	LOOPWIDTH 1	3	AUX	0	1	TRACKING 3	10
0	0	0	1	0	1	0	1	NRZC	NRZM	NRZS	INPUT CODE SØC	SØM	SØS	RZ	BP

EMR 2721 PROGRAMMING FORMAT

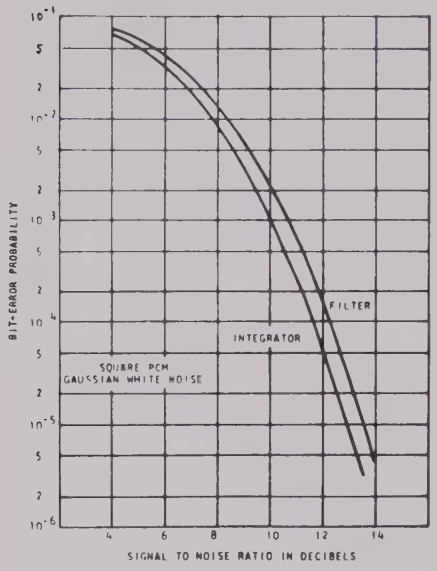
COMPUTER INTERFACE

The EMR 2721 computer interface is 16-bit parallel, for entering computer instructions, plus an additional line for the instruction transfer pulse. This interface is defined in detail in the Electrical Specifications, under the heading of "Program Instruction Inputs."

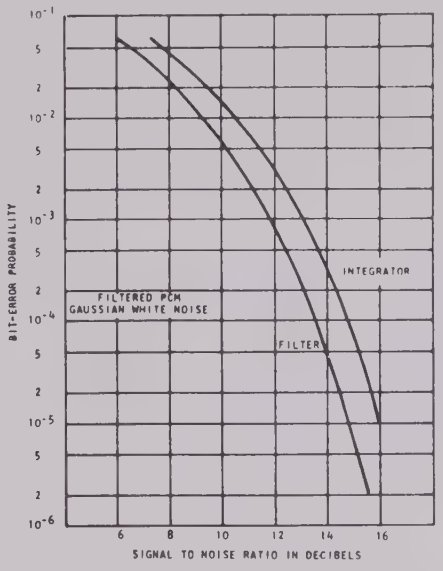
TYPICAL PERFORMANCE CURVES

The following curves are based on typical data and are provided as general PCM signal conditioning performance information.

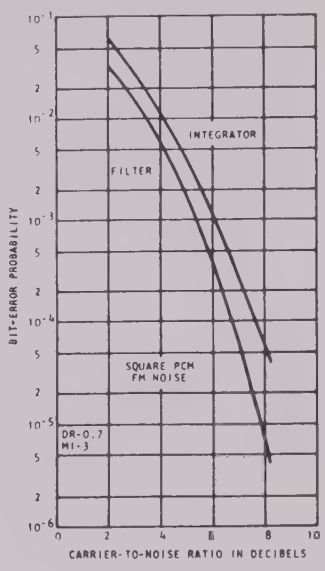
For graphs A and B the noise bandwidth is greater than 10 times bit rate. For graph C the noise is measured before the FM detector in a bandwidth corresponding to a modulation index of 3. In graph D the AC offset is a triangular waveform with a peak-to-peak amplitude equal to the peak-to-peak amplitude of the PCM.



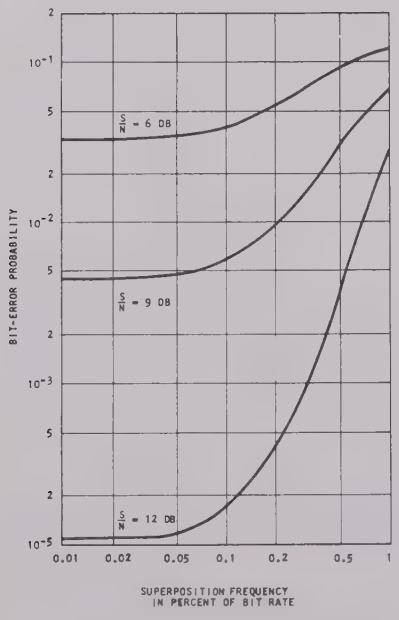
BIT ERROR PROBABILITY, SQUARE PCM WITH GAUSSIAN WHITE NOISE (TYPICAL DATA)
(A)

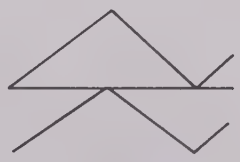


BIT ERROR PROBABILITY, FILTERED PCM WITH GAUSSIAN WHITE NOISE (TYPICAL DATA)
(B)



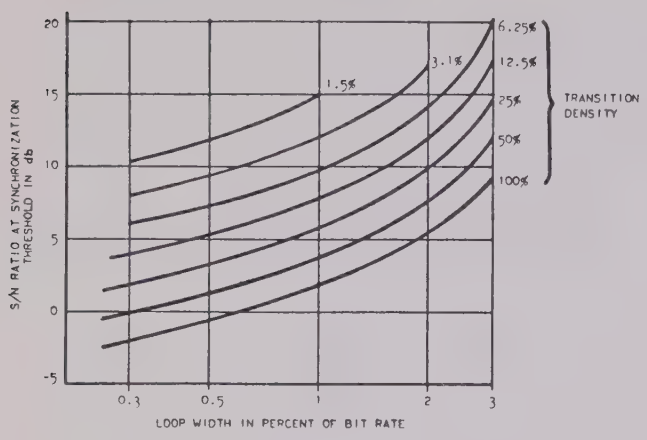
BIT ERROR PROBABILITY, SQUARE PCM WITH NOISE FROM FM DETECTOR (TYPICAL DATA)
(C)





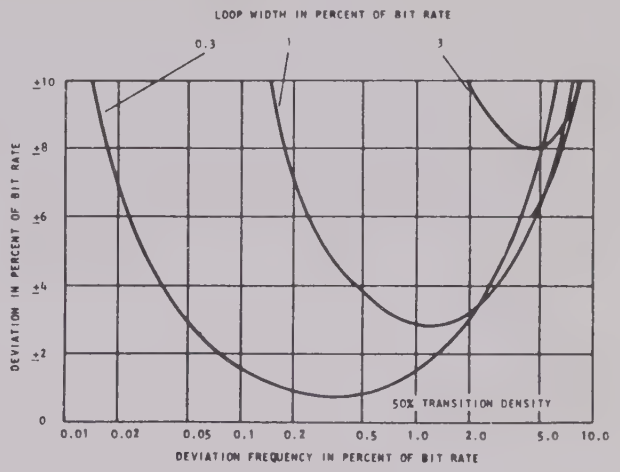
BIT ERROR PROBABILITY, AC OFFSET FREQUENCY (TYPICAL DATA)
(D)

The following curves show the typical synchronization performance of the EMR 2721. Graphs E, F, and G show the minimum signal-to-noise and maximum bit-rate variations permissable for the maintenance of synchronization. Graph H shows acquisition time in bits for differences in selected bit-rate and actual bit-rate.



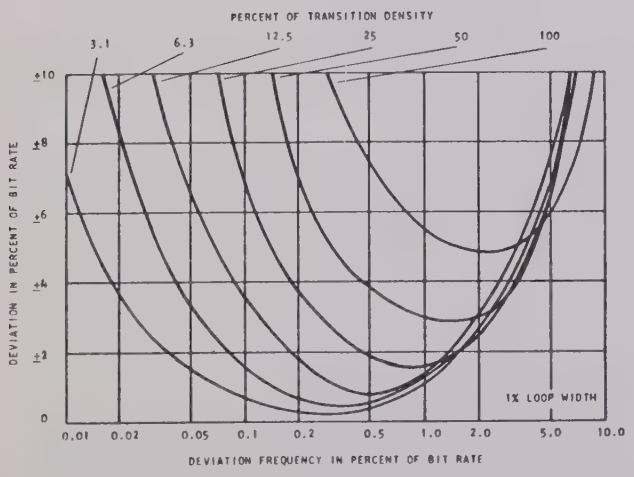
MINIMUM SIGNAL-TO-NOISE RATIO VERSUS LOOP WIDTH. DIFFERENT TRANSITION DENSITIES. (TYPICAL DATA)

(E)



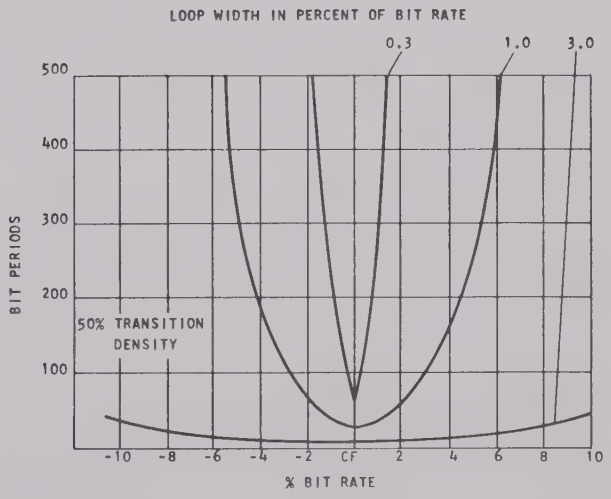
MAXIMUM BIT RATE DEVIATION VERSUS DEVIATION FREQUENCY. 50% TRANSITION DENSITY, DIFFERENT LOOP WIDTHS. (TYPICAL DATA)

(F)



MAXIMUM BIT RATE DEVIATION VERSUS DEVIATION FREQUENCY. DIFFERENT TRANSITION DENSITIES, 1% LOOP WIDTH. (TYPICAL DATA)

(G)



LOCK-IN TIME VERSUS INPUT BIT RATE. 50% TRANSITION DENSITY, DIFFERENT LOOP WIDTHS. (TYPICAL DATA)

(H)

ELECTRICAL SPECIFICATIONS

Signal Input

Codes:

NRZC, NRZM, NRZS, SØC, SØM, SØS, 50% RZ, and Bipolar accepted, as programmed.

Bit Rates:

10 bps to 1 Mbps for all codes. Required nominal bit rate programmable to 3 significant figures. Capture and tracking to ±1%, ±3% or ±10% of nominal bit rate as programmed.

Transition Density:

As low as 1 transition in 64 consecutive bit periods with a loopwidth of 0.3%, without loss of synchronization.

Levels:

0.5 to 30 volts peak-to-peak without adjustment.

Polarity:

Normal or inverted, programmable.

Configuration:

Single-ended, referenced to signal ground.

Input Impedance:

500,000 ohms resistive, or greater, shunted by a capacitance of 150 pf maximum.

Perturbations:

The EMR 2721 can accommodate the follwoing perturbations to the input signal without excessive degradation in performance:

Jitter:

Displacement of ±20% bit period, from nominal bit position.
Rate not exceeding nominal bit rate.
Non-cumulative.

AC Offset:

Amplitudes of up to 100% peak-to-peak signal level.
Frequencies of up to 0.1% nominal bit rate.
Transition density of 50% minimum.

DC Offset:

Up to 100 volts of either polarity.

Noise:

Refer to "Signal Outputs, NRZC: Bit Error Probability" and "Typical Performance Curves."

Signal Conditioning

Filter Sample:

Constant time delay filtering, program selectable for all input codes. 3db cutoff frequency (f_{co}) controlled by Bit Rate and Input Code programmed:

SØ and NRZ: f_{co} = 0.5 bit rate
RZ: f_{co} = Bit rate

Reset Integrator:

Program selectable for all input codes.
Time constant controlled by Bit Rate programmed.

Signal Outputs

NRZC:

Serial. Always NRZC, provided that correct input code and polarity have been programmed.

Logic Levels: "1" = 3 to 5v
"0" = 0 to 0.45v
Single rail logic with separate ground

Drive Available: 12 TTL unit loads i.e.:

Logic "1": 1.2ma maximum at 4.5v to the loads.

Logic "0": 20ma maximum at 0v from the loads.

Rise and Fall Times: 0.1 μs maximum.

Recorder:

Serial NRZC, NRZM or SØC as programmed, and independent of input code, provided that the correct input code and polarity have been programmed.

Level:

2 volts peak-to-peak ±20%, centered about signal ground within ±20% of the peak-to-peak value.

Drive Available:

50-ohm coaxial cable terminated with a 50-ohm ±10% resistive load.

Rise and Fall Times:

0.25 μs maximum.

Bit Error Probability:

No greater than the figures shown in the following table for all codes when the PCM signal is embedded in gaussian white noise with a bandwidth greater than 10 times bit rate.

S/N Ratio (db)	Square PCM with a Reset Integrator Detector	Filtered PCM at 0.75 Bit Rate with a Filter-Sample Detector
3	6×10^{-2}	9×10^{-2}
6	1.2×10^{-2}	4×10^{-2}
9	8×10^{-4}	1×10^{-2}
12	4×10^{-6}	7×10^{-4}

The signal is defined as 1/2 peak-to-peak voltage level with the PCM at a stable bit rate and a 50% transition density.

The noise is defined as the RMS noise voltage measured in, or referred to, a bandwidth of 1/2 bit rate for all NRZ and SØ codes, and a bandwidth of bit rate of RZ and Bipolar codes.

Bit Synchronization

Acquisition Time:

Less than 100-bit periods for a capture range of ±10% and a loop width of 3%.

Capture and Tracking Range:

±1%, ±3%, or ±10% of nominal bit rate, as programmed.

Loop Filter Width:

0.3%, 1%, or 3% of nominal bit rate, as programmed.

Bit Rate Outputs

Four separate pulse train outputs, synchronous with the NRZC and recorder serial PCM outputs as follows:

0^{o} Clock:

Positive-going edge in phase with the beginning of a bit period.

90^{o} Clock:

Positive-going edge occurring after 1/4-bit period.

180^{o} Clock:

Positive-going edge occurring at mid-bit time.

270^{o} Clock:

Positive-going edge occurring after 3/4-bit period.

Levels:

Pulse = 3 to 5v

No Pulse = 0 to 0.45v

Pulse Duration:

1/2-bit period.

Rise and Fall Times:

0.1 μs maximum.

Program Instruction Inputs

Programmable Functions:

All adjustable functions i.e.: bit rate, input polarity, type of detection (sample, filter sample, reset integrator), recorder output code, phase-locked loop width and tracking range, input code.

Mode of Entry:

Local Control: Front panel Local Programming switches.

Remote Control: Computer interface lines.

Instruction Format:

16-bit word, in common with all EMR 2700 Series units, contains the following fields:

Module Address:

For remote control only. 4-bit field, selectable by means of internal jumper wires allows the EMR 2721 to be addressed and programmed from a remote source.

Group Address:

4-bit field specifies the function to be programmed. (3 bits used for the EMR 2721.)

Instruction:

8-bit field contains the required function parameter to be entered into the storage registers.

Transfer Pulse:

1 line, a "1" for 1- to 5-μsec duration. This pulse effects entry of the instruction word.

Logic Levels:

"1" = 1.9 to 5v
"0" = 0 to 1.1v
Single rail logic with separate ground for each signal.

Drive Required:

Each input line represents one TTL unit load, i.e.:

Logic "0": 1.66ma maximum at 0v to the remote circuit.

Logic "1": 0.1ma maximum at +4.5v from the remote circuit.

Displays

Stored Instructions:

The contents of all instruction storage registers are displayed on the front panel, grouped under appropriate function titles.

Meters:

Two edgewise meters are provided.

Input:

Indicates the peak-to-peak input signal level with two ranges: 0 to 10v and 0 to 30v. Required range automatically selected and indicated.

Deviation:

Indicates percentage deviation of input bit rate from nominal.

Indicator Lamps:

Three indicator lamps are provided.

Sync:

Indicates loss-of-lock condition.

30V and 10V:

Two lamps to indicate the peak-to-peak voltage range of the Input meter.

Lamp Test:

A pushbutton tests all display lamps.

Power Requirement:

115v rms or 120v rms, ±10%, 47 to 65 Hz, single phase (180 watts at 120 volts).

MECHANICAL SPECIFICATIONS

Panel Size: 5-1/4 in. H by 19 in. W (13.3 by 48.2 cm).

Overall Depth: 22 in. (55.9 cm), excluding projections from front panel.

Weight: Net, 55 pounds (24.95 kg). Shipping, 70 pounds (31.75 kg).

Panel Finish: A combination of light and dark green semigloss baked enamel with white lettering is standard. Other panel and lettering paints are available on request.

Mounting: Slides and hardware for installation in an EIA-type rack are provided.

ENVIRONMENTAL SPECIFICATIONS

Temperature: Operating, $0^{o}C$ to $+50^{o}C$. Non-Operating, $-40^{o}C$ to $+85^{o}C$.

Relative Humidity: Operating and non-operating, 5% to 95%.

Altitude: Operating and non-operating, up to 10,000 feet.

Shock: Non-operating - MIL-STD-810A, Method 516 Procedure I, (20g for 10 millisecs).

Vibration: Non-operating - MIL-STD-810A, Method 514 Equipment Class 6, Fig. 514-6 Curve A. Or, will meet MIL-STD-167.

TELEMETRY DIVISION

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